SuitSat 2 Experiment Proposal

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Kettering University

- Kettering University
  - private university in Flint, MI
  - focuses on undergraduate education, mostly in engineering
  - approximately 2,200 students
- Kettering is known for
  - extensive co-op program
    - engaging students in industry from their freshman through senior years
    - culminates in a Bachelors thesis
  - real-world, applicable approach to teaching
  - produces students that are extremely capable in the workplace
- Additional information can be found at *www.kettering.edu*

Project Proposal

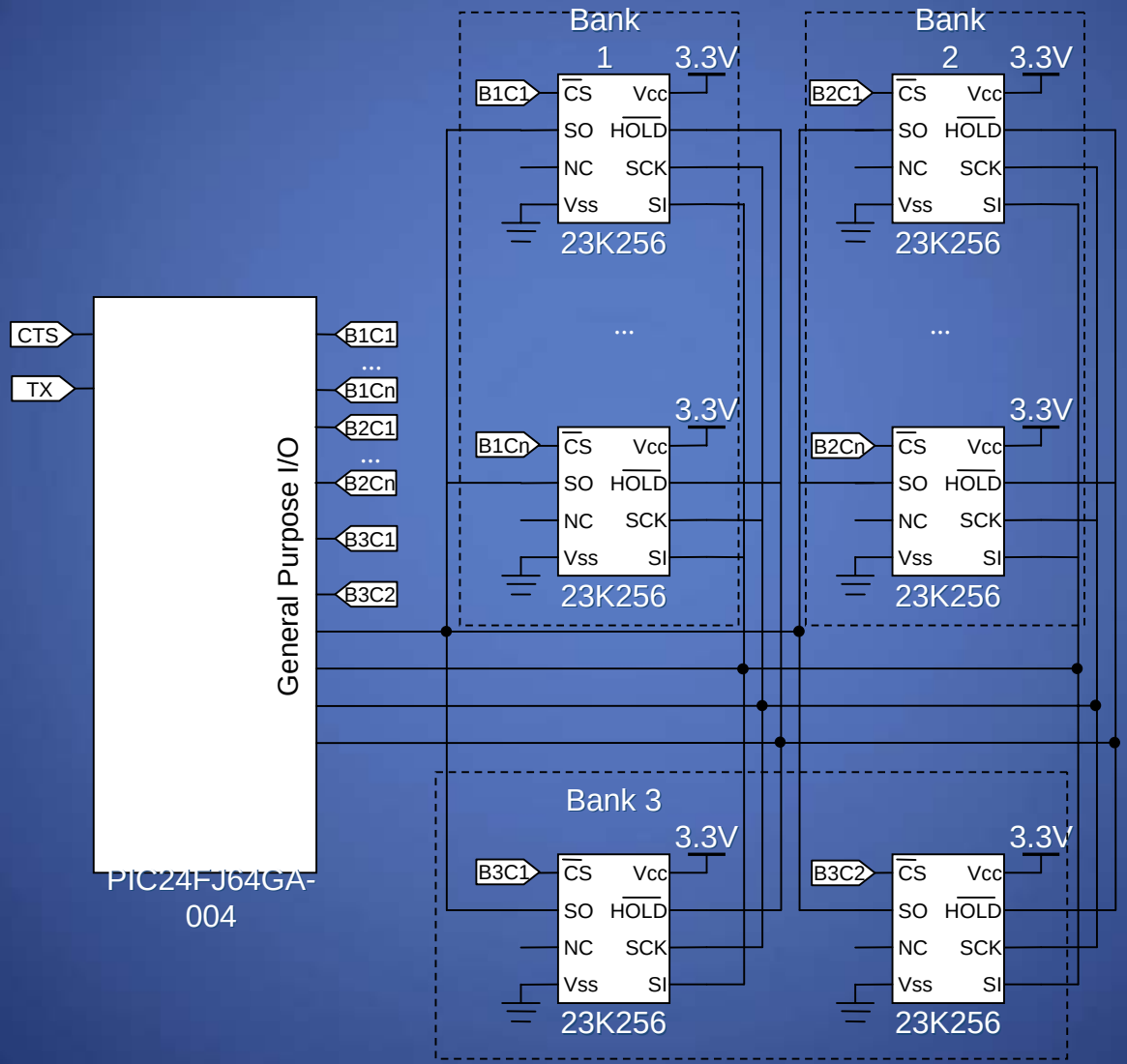
- Hardening of integrated circuits to protect against radiation in space environments is a well known topic.
- To explore the need for this added protection, this project will measure the rate of single event effects (SEE) on unhardened commercial off-the-shelf (COTS) SRAMs to observe the protection provided by the space suit.

Approach:

- Use an array of Microchip 23K256 SRAM chips for a maximal sensitive cross-sectional area.
- Monitor single event upsets (SEU) that occur in stored data and errors from single event transients (SET) that occur as data is read from and written to the SRAM.

➢ Evaluate the susceptibility of COTS parts exposed to an actual space environment instead of simulated conditions or mathematical models.

Project Block Diagram



SRAM Banks 1 and 2

- Used to detect SEU or SET during reads.
- Each bank is initialized with a specific bit pattern every time the system regains power.
- Each bank is periodically scanned to verify the SRAM contents, and a counter is used to track the amount of time the chips were exposed to radiation since the latest reset.
  - Counter set to 0 upon a system reset, which rewrites values to the SRAM.
- If a new error occurs in a read, the memory location is reread.
  - If the error persists, the stored value has changed and an SEU event is logged.
  - Otherwise, an SET read event is logged due to the initial read error.
- Each bank is tentatively ten 32kB Microchip 23K256 SRAM devices.
  - 3.3 V operation
  - 4 uA standby current with 3 mA needed to access the device with a 1 MHz SPI interface

SRAM Bank 3

- Used to detect SETs during reads or writes.
- A bit pattern is written to the bank, then the bank is read to verify contents.
- If an error occurs during a read, the memory location is reread.
  - If the error persists, a write SET event is logged.
  - Otherwise, an SET read event is logged due to the initial read error.
- The number of complete read/write scans is maintained in a counter and is logged when an error occurs.
  - Write counter saved in Flash and persists through a power reset
- Bank 3 uses two Microchip 23K256 devices, one primary and one backup.

Reliable Operation

The following features allow the project to operate correctly without intervention and/or return to a default working state after power is cycled.

- Two copies of program code
  - Watchdog timer and program checksums are used to verify correct operation and determine which copy to use
- Initialized bit pattern in Flash
  - Stores specific pattern in Flash during the first startup
  - Presence or absence of pattern selects one-time startup code or power-cycle code
- Experiment data stored in Flash
  - Two copies stored in redundant tables
  - Each log entry contains a checksum to indicate corrupted data
- Write counter stored in Flash in triplicate
  - Each of the three copies is stored in a different Flash line and updated independently
  - System compares values after a power cycle and will always have at least two

Project Communication

The project's one-way communication with the SuitSat 2 system:

- It will send a short message containing the number of logged events then transmit the event logs one by one as long as the CTS signal is asserted.
- Each log entry contains its own checksum and is stored twice in Flash, protecting against errors in the log itself and preserving data if power is lost.
- Contents of the event log entries are shown on the next slide.
- Note: Log entries are 9 bytes, corresponding to three 3-byte PIC program instructions worth of Flash.

Event Log Formats

Byte	Banks 1 and 2 SEU or SET Read Error	Bank 3 SET Read or Write Error	Program Code Error SEU Error
1	Read Tick Counter High	Write Counter High	Write Counter High
2	Read Tick Counter Low	Write Counter Middle	Write Counter Middle
3	Chip Number	Write Counter Low	Write Counter Low
4	Bank Number	Bank Number	Program Number
5	Memory Address High	Memory Address High	Memory Address High
6	Memory Address Low	Memory Address Low	Memory Address Middle
7	Memory Contents	Memory Contents	Memory Address Low
8	Error Type	Error Type	Memory Contents
9	Checksum	Checksum	Checksum

Project Overview

- Funding: minimal (less than $200) provided by existing, available Kettering faculty grants
- Development Time: 3 to 4 weeks (development using the SuitSat 2 evaluation board has already begun)
- Communication: Download of logged events using the SuitSat 2's specified protocol.
- Certification Requirements: none
- ISS Crew Involvement: none
- ISS Resources Required: none
- Operating Procedures: none

Principle Investigators

The two people working on this project are Dr. David Foster and Dr. Girma Tewolde. Both are heavily involved in the microcomputers courses taught in the Electrical and Computer Engineering Department at Kettering University.

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