



TP1[8:0] → TP1[8:0]

FF5 is reset by the same signal that resets FF1  
 FF5 is set by the falling edge of nWDOVF, which  
 causes a reset. Use of FF5 protects the system from  
 a stuck level on the input pin.

This diagram shows the self-timing completion of the nRST pulse.  
 The time from removal of PONRESET to assertion of CTR2\_12 Q[1] is not to scale.  
 nRST lasts 3 cycles of 6400 Hz, or 469 uSec, when triggered by CTR2\_12 as shown.  
 It could last up to 4 cycles, or 625 uSec, if triggered by EXTRSTA or B, as they are  
 asynchronous events to the 6400 Hz clock.  
 Normally, PNT127W will be triggered by the pattern from WDOG DAT, clearing CTR2\_12  
 thus preventing resets.

CTR2\_12 Q[1]  
 PONRESET  
 CLK6400HZ  
 FF1 Q  
 nRST  
 FF2 Q  
 FF3 Q  
 FF4 Q

nRST changed to RST (polarity change).  
 ENABLE changed from PNT127 blocks to CTR2\_12 block.  
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**QuickLogic**  
 Corporation  
 1277 Orleans Drive  
 Sunnyvale, CA 94089  
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