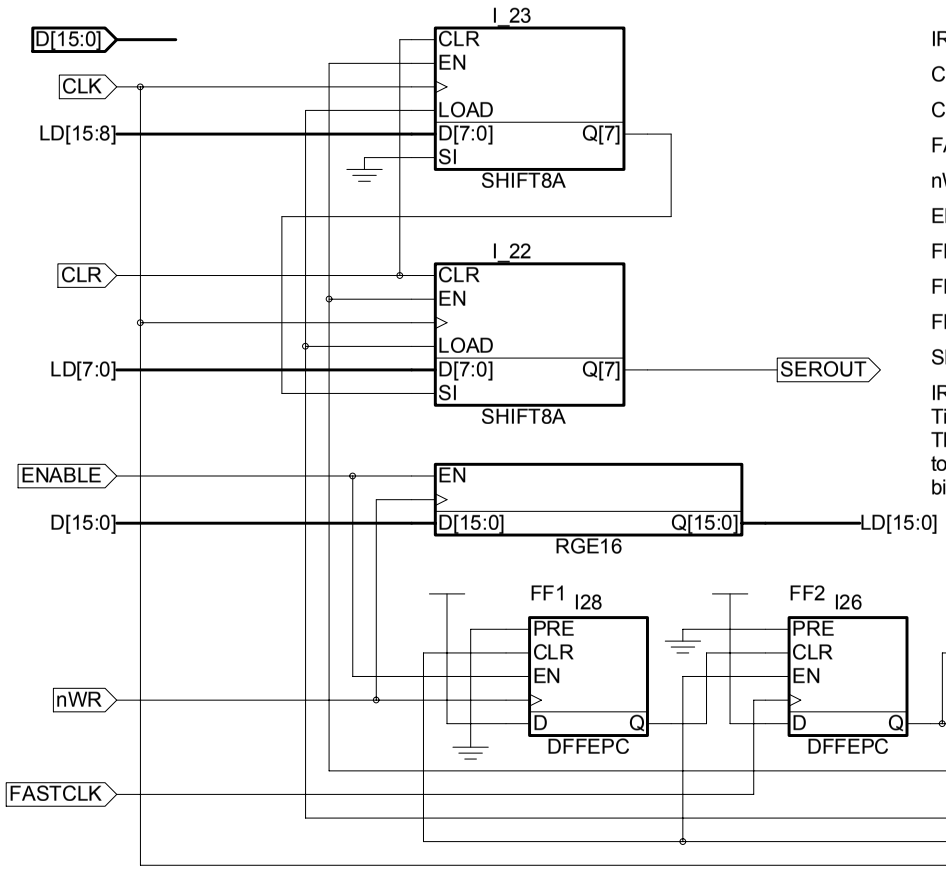

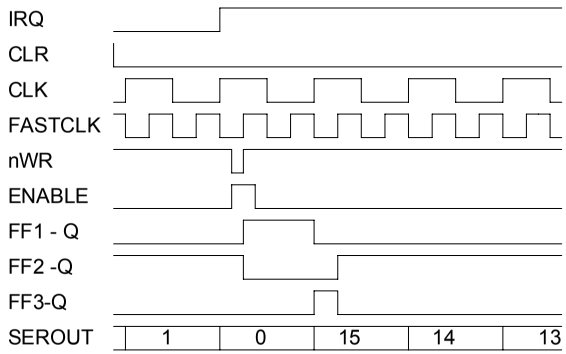

IRQ assertion is assumed, and is for reference only.
Timing relationships nWR and ENABLE are not to scale.
They are asynchronous to the clocks. FF1-3 are used
to synchronise the loading of the shift registers. SEROUT values are
bit weights, sequencing from the MSB to the LSB.

QuickLogic Corporation 1277 Orleans Drive Sunnyvale, CA 94089	SR16WPRE	
	SR16WPRE	
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