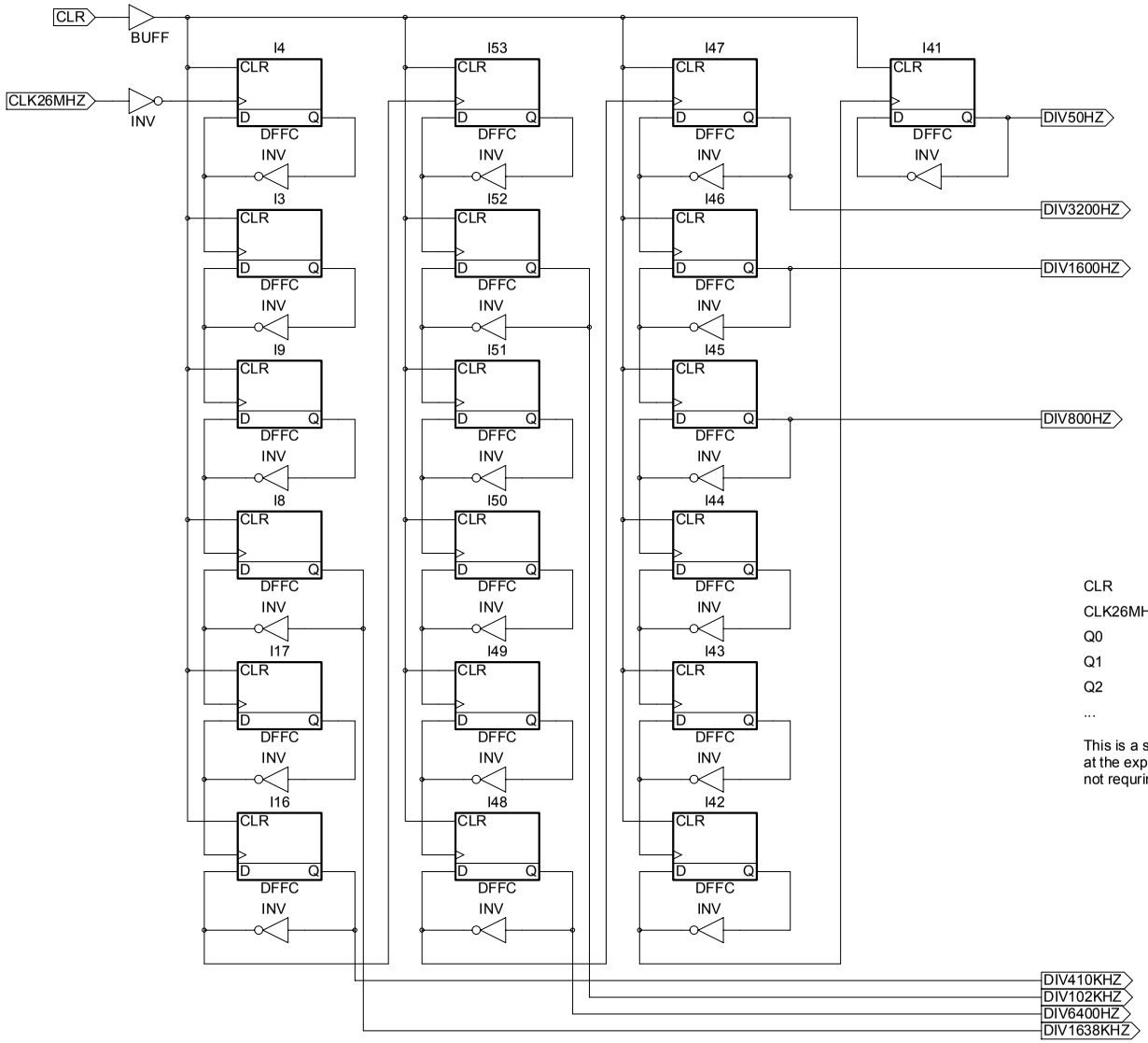

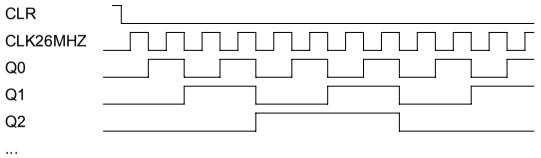

This is a simple ripple counter. This architecture minimises power consumption at the expense of increased propagation delay. It also has the benefit of not requring a low-skew clock network inside the QuickLogic FPGA.

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